Claims

[c1] 1.A multi-memory architecture with an externally accessible storage capacity known as a total memory capacity and the number of pins of the multi-memory architecture having the total memory capacity is known as a total pin number, wherein the total pin number comprises used and unused pins, the multi-memory architecture comprising:a first memory device having a first data storage capacity and a first predefined pin configuration having a first number of pins which is the actual number of used pins according to the first data storage capacity; and
a second memory device having a second data storage capacity and a second predefined pin configuration having a second number of pins which is the actual number of pins according to the second data storage capacity;wherein the first number of pins is greater than the second number of pins, and the total number of pins of the multi-memory architecture is not less than the number of pins of the first memory device of multi-memory architecture having the total memory capacity.

[c2] 2.The multi-memory architecture of claim 1, wherein the externally-accessible total data storage capacity of the multi-memory architecture is equal to the data storage capacity of the first memory device plus the data storage capacity of the second memory device.

[c3] 3.The multi-memory architecture of claim 1, wherein the second memory device comprises a plurality of segments and each segment has a data storage capacity equal to the data storage capacity of the first memory device; wherein the storage space of the first memory device is used to replace one of the segments in the second memory device so that an access to the replaced segment is mapped to the storage space of the first memory device.

[c4] 4.The multi-memory architecture of claim 3, wherein the segment in the second memory device that is currently being replaced by the first memory device is used to replace any one of the segments in the second memory device other than the one currently being replaced by the first memory device.

[c5] 5.The multi-memory architecture of claim 3, further comprising: at least one

replacement segment in the second memory device, whose data storage capacity equals to each segment in the second memory device is used to replace any one of the segments in the second memory device other than the one being currently replaced by the first memory device.

[c6] 6.The multi-memory architecture of claim 1, further comprising a replacement memory area, whose data storage capacity equals to the second memory device, which is partitioned into a plurality of segments each being equal in data storage capacity to the first memory device; the replacement memory area is used to replace the second memory device to allow the externally-accessible total storage space of the multi-memory architecture to cover the currently-accessed memory device selected from the second memory device, the replacement memory area excluding the storage space of the segment currently being replaced by the first memory device, and the first memory device in some segments of the currently-accessed memory.

[c7] 7.The multi-memory architecture of claim 6, wherein the segment currently being replaced by the first segment is replaced by any one of the segments in the currently-accessed memory device other than the one being currently replaced by the first memory device.

[c8] 8.The multi-memory architecture of claim 6, wherein the second memory device further comprising a plurality of second memory replacement segments, each being equal in data storage capacity to each segment in the currently-accessed memory device, which is used to replace any one of the segments in the currently-accessed memory device other than the segment currently being replaced by the first memory device.

[c9] 9.The multi-memory architecture of claim 1, wherein the pin configuration of the first memory device having a total data capacity which is the sum of the first and second data capacities.

[c10] 10.A multi-memory architecture comprising:
a first memory device having a first data storage capacity; and
a second memory device having a second data storage capacity;

wherein
an overall pin configuration of the multi-memory architecture is compatible with the pin configuration of the first memory device having the second data storage capacity.

[c11] 11.The multi-memory architecture of claim 10, wherein the externally-accessible total data storage capacity of the multi-memory architecture is equal to the data storage capacity of the first memory device plus the data storage capacity of the second memory device.

[c12] 12.The multi-memory architecture of claim 10, wherein the second memory device includes a plurality of segments and each segment comprises a data storage capacity equal to the data storage capacity of the first memory device; wherein the storage space of the first memory device is used to replace one of the segments in the second memory device so that an access to the replaced segment is mapped to the storage space of the first memory device.

[c13] 13.The multi-memory architecture of claim 12, wherein the segment in the second memory device that is currently being replaced by the first memory device is used to replace any one of the segments in the second memory device other than the one currently being replaced by the first memory device.

[c14] 14.The multi-memory architecture of claim 12, further comprising: at least one replacement segment in the second memory device, whose data storage capacity equals to each segment in the second memory device, which can be used to replace any one of the segments in the second memory device other than the one being currently replaced by the first memory device.

[c15] 15.The multi-memory architecture of claim 10, further comprising a replacement memory area, whose data storage capacity equals to the second memory device, which is partitioned into a plurality of segments each being equal in data storage capacity to the first memory device; the replacement memory area is used to replace the second memory device to allow the externally-accessible total storage space of the multi-memory architecture to cover the currently-accessed memory device selected from the second memory

device and the replacement memory area excluding the storage space of the segment currently being replaced by the first memory device, and the first memory device in some segments of the currently-accessed memory.

[c16] 16.The multi-memory architecture of claim 15, wherein the segment currently being replaced by the first segment is replaced by any one of the segments in the currently-accessed memory device other than the segment being currently replaced by the first memory device.

[c17] 17.The multi-memory architecture of claim 15, wherein the second memory device further includes a plurality of second memory replacement segments, each being equal in data storage capacity to each segment in the currently-accessed memory device, which is used to replace any one of the segments in the currently-accessed memory device other than the segment currently being replaced by the first memory device.

[c18] 18.The multi-memory architecture of claim 10, wherein the pin configuration of the first memory device having a total data capacity which is the sum of the first and second data capacities.

[c19] 19.A memory access controller for use in the multi-memory architecture composed of a first memory device and a second memory device comprising;
a segment identification unit, which is capable of generating a memory-access control signal in response to an input address signal;
a command identification unit, which is capable of generating a memory-mode signal in response to an input control signal; and
a memory selection unit, which is used to select between the two memory devices in the multi-memory architecture based on the memory-access control signal and the memory-mode signal.

[c20] 20.The memory access controller of claim 19, wherein the segment identification unit includes:
a first memory address register for the first memory device, which is used to store a set of data representative of the address of the first memory device; and
a first comparator, which is capable of comparing an input address signal

against the content of the first memory address register to thereby generate the memory-access control signal.

[c21] 21.The memory access controller of claim 19, further comprising:
a replaced-segment register, which is used to store the address of the segment in the second memory device of the segment of the second memory device that is to be replaced by the first memory device;
a second comparator, which is capable of comparing the input address signal against the content of the replaced-segment register; if matched, the second comparator outputs an enable signal;
a virtual-segment register, which is used to store the address of the first memory device; and
a multiplexer module, which is under selection control by the enable signal output from the second comparator for selectively transferring either the content of the virtual-segment register or the segment access code in the input address signal to a decoder.

[c22] 22.The memory access controller of claim 21, further comprising an interface circuit coupled to the first memory address register, the replaced-segment register, and the virtual-segment register for altering the content of a selected register therefrom.

[c23] 23.The memory access controller of claim 21, further comprising a group of address buffers for storing the segment access code for identification of the address of the first memory device in the input address signal.

[c24] 24.The memory access controller of claim 19, further comprising:
a replaced-segment register, which is used to store the address data indicating the segment in the second memory device that is currently being replaced by the first memory device;
a second comparator, which is capable of comparing the input address signal against the content of the replaced-segment register; if matched, the second comparator outputs an enable signal;
a swap-segment register, which is used to store the address of the address of the first memory device and a tag of a replacement memory area being swapped

to replace the second memory device; and
a multiplexer module, which is under selection control by the enable signal output from the second comparator for selectively transferring either the content of the swap-segment register or the segment access code in the input address signal to a decoder.

[c25] 25.The memory access controller of claim 24, further comprising an interface circuit coupled to the first memory address register, the replaced-segment register, and the swap-segment register for altering the content of a selected one therefrom.

[c26] 26.The memory access controller of claim 24, further comprising a group of address buffers for storing the segment access code for identification of the address of the first memory device in the input address signal.